Design and Analysis of Ternary Logic Gates and Combinational Circuits in 180nm CMOS

Soumita Haldar Chakraborty, Suman Haldar

Abstract— The multi-value logic system specifically the ternary logic system can be a good alternative in processing of digital signals and high speed data transfer in optical communication based systems. This paper presents design, implementation and analysis of Ternary logic gates and combinational circuits have been validated using Tanner EDA tool .We have developed a simplified ternary multiplexer and decoder circuit that accounts for a intermediate voltage level. The power dissipation, waveform and transient delay analysis of ternary logic gates and combinational circuits have been presented in detail.

Index Terms- Multi valued logic (MVL), Positive Ternary Inverter (PTI),Standard Ternary Inverter(STI),Ternary logic, Ternary Digits(TRITS), Negative Ternary Inverter(NTI), TRITS Interval

1. INTRODUCTION

A ternary, three-valued or trivalent logic is one of several MVL [1],[2] systems. In a ternary system, three logic levels are used (0, 1, 2) corresponding to low, middle and high voltage level.The Boolean arithmetic using ternary logic [3],[4] had already been developed. Ternary logic or three valued logic provides several advantages over binary logic in the design of digital systems [5],[6]. Such advantages include more information in a given register length and higher speed of operation during arithmetic and logical operations. As the hardware requirement of a ternary circuit is less in comparison to the binary counterpart, ternary circuits can be implemented with reduced complexity of interconnects and less chip area resulting speed enhancement [7] and significant reduction of static power dissipation. There are many applications of the ternary (three-value) logic circuits. For example, in an N bit processor, the number of bits per word that needs to be stored is N^2, whereas in case of ternary logic, the number of bits per word should be $N * \log_3 2$. A Ternary logic offers better utilization of transmission channels because of the higher information content carried by each line, also gives more efficient error detection and correction codes and possess potentially higher density of information storage.

2. TERNARY LOGIC GATES

2.1 Ternary Inverter

The ternary inverter [1] is broadly classified into three categories namely negative ternary inverter (NTI), standard ternary inverter (STI) and positive ternary inverter(PTI).In a Negative ternary inverter if input X=0,1and 2 then output will be Y_0=2, 0 and 0 respectively.so the mathematical expression is

$$Y_0 = C_0(x) = 2 \text{ if } x = 0 \quad (1)$$
$$= C_0(x) = 0 \text{ if } x \neq 0$$

In a Standard or simple ternary inverter if input X=0,1and 2 then output will be Y_0=2, 1 and 0.so the mathematical expression is

$$Y_0 = C_1(x) = 2 - x \quad (2)$$

In Positive ternary inverter if input X= 0,1and 2 then output will be Y_0=2, 2 and 0 so the mathematical expression is

$$Y_0 = C_2(x) = 2 \text{ if } X \neq 2 \quad (3)$$
$$= C_2(x) = 0 \text{ if } X = 2$$

2.2 Ternary Nand Gate

A general ternary NAND (GTNAND) is a device with two inputs $X_1$and X_2 and three outputs Y_0, Y_1 and Y_2 such that

$$Y_i = C_i(Z) \quad (4)$$

Where Z=min (X_1, X_2) for i=0, 1or 2. If output is taken to be Y_0, Y_1, or Y_2, the device is said to as a negative ternary NAND (NTNAND), a standard ternary NAND (STNAND), or a positive ternary NAND (PTNAND) respectively.Truth table of ternary nand gate is illustrated in table 1.

2.3Ternary Nor Gate

A general ternary NOR (GTNOR) is a device with two inputs X_1 and X_2 and three outputs Y_0, Y_1 and Y_2 such that

$$Yi = Ci\ (Z)$$

Where Z=max (X_1, X_2) for i=0, 1or 2.If output is taken to be Y_0,Y_1,orY_2,the device is said to as a negative ternary NOR (NTNOR), a standard ternary NOR (STNOR), or a positive ternary NOR (PTNOR) respectively. Truth table of ternary nand gate is depicted in table 2.

3. TERNARY COMBINATIONAL CIRCUIT

3.1 Ternary Decoder

A 1:3 decoder has one input(X) and three outputs X_0,X_1 and X_2.The ternary decoder generates unary functions for an input X to 3^X unique output lines, such that each output line will be activated for only one of the possible combination of inputs.So

Soumita Haldar Chakraborty is currently attached with dept of electronics and communication engineering in Neotia Institute of Technology Management and Science,India,PH-8145917560. E-mail: soumita.haldar@ rediffmail.com
Suman Haldar is currently attached with dept of electronics and communication engineering in Neotia Institute of Technology Management and Science,India,PH-9830378118. E-mail: suman_hldr79@ rediffmail.com

the logical expression of ternary 1:3 decoder can be written as

$$X_0 = 2(X^0)$$
$$X_1 = 2(X^1) \quad (5)$$
$$X_2 = 2(X^2)$$

The response of the ternary decoder [8] to the input X is given by

$$X_i = 2 \quad \text{if } X = i \quad (6)$$
$$= 0 \quad \text{if } X \neq i$$

3.2 Ternary Multiplexer

The ternary multiplexer has three select line and one output as compared to conventional binary multiplxer.Corresponding selection of ternary digits as a 0,1 and 2 one out of three data line I_0, $I_1$and I_3 is selected. The proposed multiplexer is implemented using decoder and STNAND (Standard Ternary NAND) instead of STNOR.

The logic expression of the multiplexer can be expressed as

$$Y = I_0 \quad \text{for } S_0 = 0$$
$$Y = I_1 \quad \text{for } S_1 = 1 \quad (7)$$
$$Y = I_2 \quad \text{for } S_2 = 2 .$$

TABLE 1
TRUTH TABLE OF TERNARY NAND GATE

Input		Output		
X_1	X_2	Y_0	Y_1	Y_2
0	0	2	2	2
0	1	2	2	2
0	2	2	2	2
1	0	2	2	2
1	1	0	1	2
1	2	0	1	2
2	0	2	2	2
2	1	0	1	2
2	2	0	0	0

TABLE 2
TRUTH TABLE OF TERNARY NOR GATE

Input		Output		
X_1	X_2	Y_0	Y_1	Y_2
0	0	2	2	2
0	1	0	1	2
0	2	0	0	0
1	0	0	1	2
1	1	0	1	2
1	2	0	0	0
2	0	0	0	0
2	1	0	0	0
2	2	0	0	0

4. SIMULATION RESULT

4.1 Ternary Inveter

In case of PTI, when input X reaches to - 2.5 volt (logic 0) then output reaches to +2.5 volt (logic2) because at this time pmos is turned on, since this path acts like close path the total voltage drop appears at the output terminal is +2.5 volt. When input X =0 volt or (logic 1) then output equals to + 2.5 volt or appeared as a logic 2.When input appears as a +2.5 volt or as a logic 2 the pmos gate to source terminal is open.As a result output appears as a -2.5volt (logic 0).PMOS transistor was simulated with a threshold volatge as specified by the TSMC 180nm design parameter.

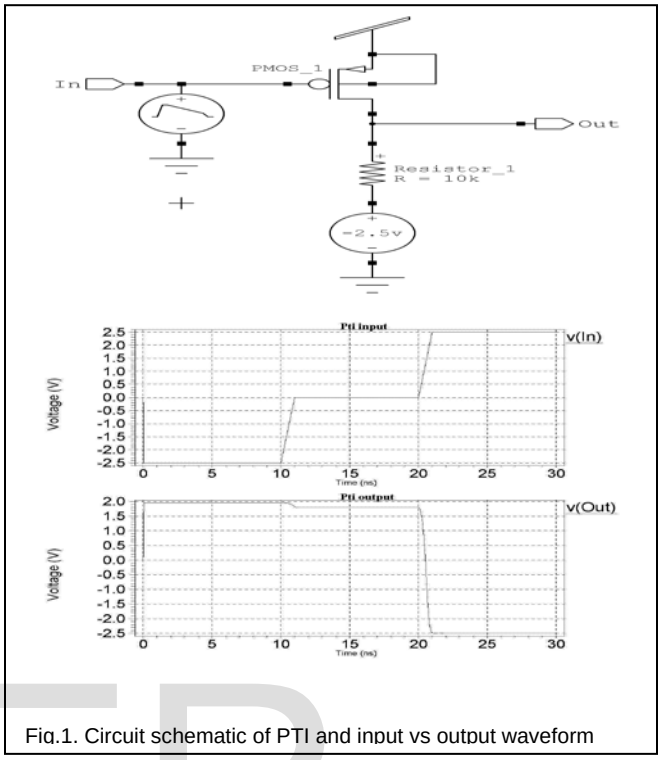

Fig.1. Circuit schematic of PTI and input vs output waveform

4.2 Ternary Nand Gate

The circuit diagram of negative ternary nand is shown in figure.2.Both the inputs X_1 and X_2 are maintained to -2.5 volt as a logic 0.The PMOS transistors are conducting state and NMOS are in OFF state. As a result output Y_0 is maintained 2.5 volt as a logic 2. The output Y_0 reaches to -2.5 volt (logic 0) for a input combination of logic 1 due to conduction of NMOS and PMOS.

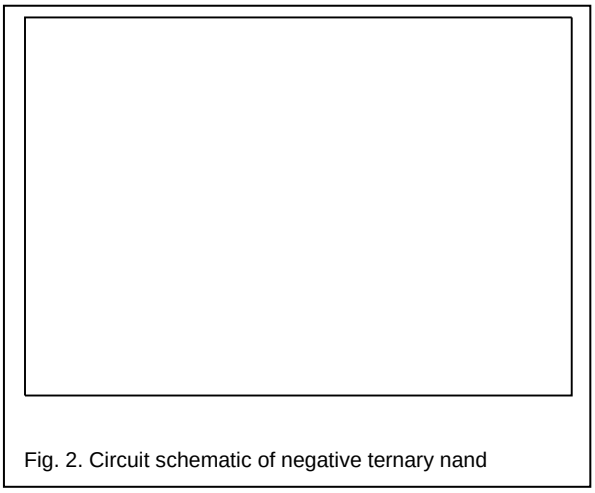

Fig. 2. Circuit schematic of negative ternary nand

The input and output waveform of negative ternary nand for 10 ns TRITS interval is shown in figure.3.It has been observed from simulation that for a different TRITS input combination output waveform Y_0 follows the same result shown in table 1.

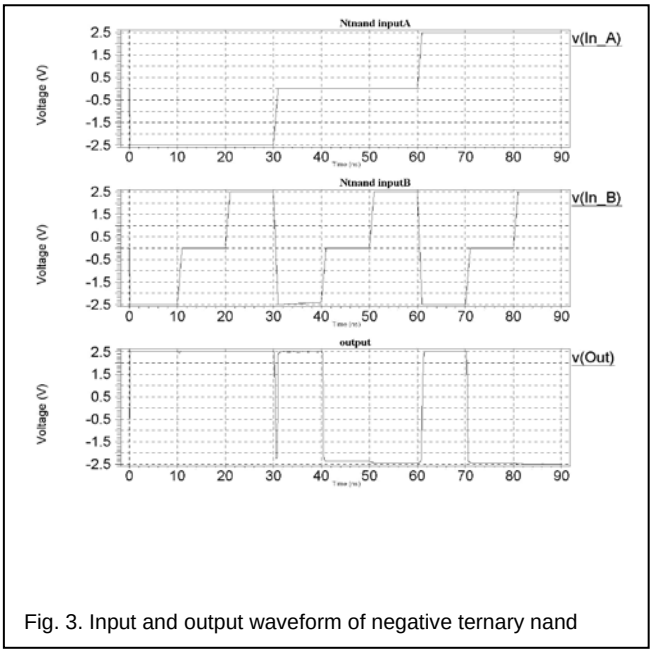

Fig. 3. Input and output waveform of negative ternary nand

4.3 Ternary Nor Gate

The circuit schematic of 2 input negative ternary NOR is shown in figure 4.The TRITS interval is taken as a 10 ns for both the inputs.According to this configuration when both the inputs are logic 0 ie,TRITS are maintained at -2.5 voltage level, the output will be logic 2 due to switching on behavior of PMOS.Except this set of combination the output shows logic 0.From the figure.5 it is clear that output of NTNOR follow the truth table listed in Table2.

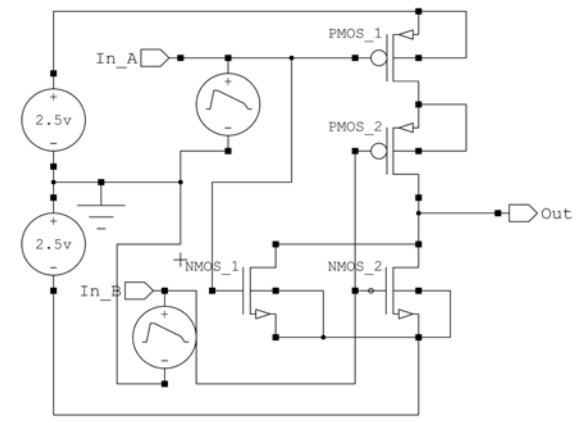

Fig.4.Circuit schematic of negative ternary nor

5. SIMULATION RESULT OF COMBINATIONAL CIRCUIT

5.1 Ternary Decoder

Using equation 6. the ternary docoder is implemented using two NTI , one PTI and one NTNOR gate.As shown in figure 6 the output of two NTI gates are considered as a decoder output A and C respectively.Both the NTI output is fed to NTNOR to produce a output B.

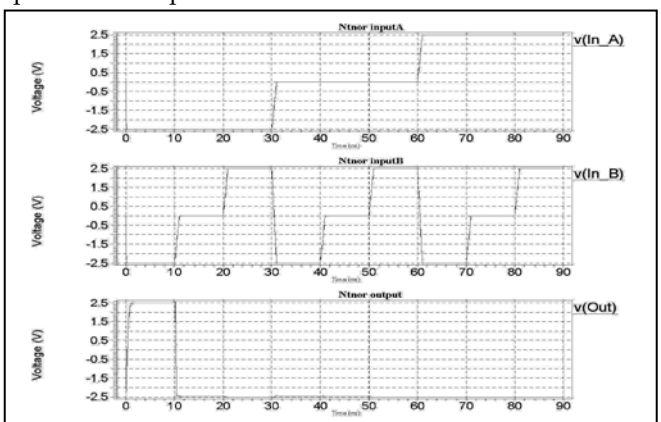

Fig.5 Input and output waveform of negative ternary nor

The input and output characteristics of ternary decoder is shown in figure.7.TRITS interval is taken as 30 ns for ternary logic 0,1 and 2 respectively.

From the circuit schematic shown in fig.6 it is clear that when -2.5 volt is applied for 30ns trits interval as a logic 0 the output of NTI and PTI produces logic 2.The output A from first NTI is maintained at logic 2.The PTI output is followed by a input of second NTI producing logic 0 from output C. Both the output taken from NTI is considered as a input to NTNOR.As a result logic 0 is appeared as an output B of NTNOR .

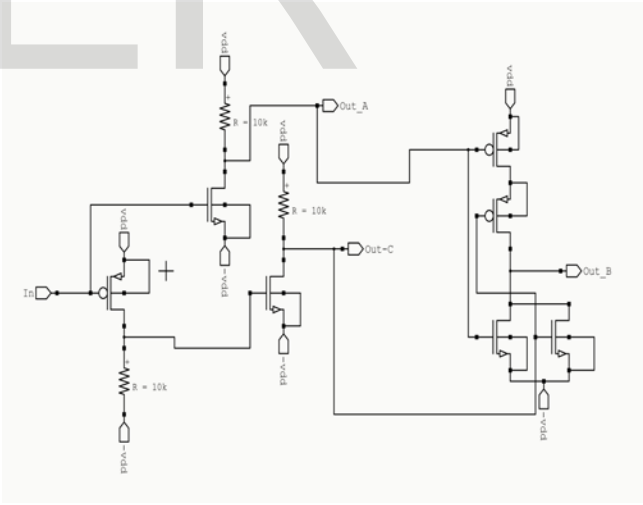

Fig.6.Circuit schematic of ternary decoder

As shown in figure.7 the output of decoder produces logic 2 once at a time for a given TRITS interval of 30ns for logic 0,1and 2 respectively. It can be realized from switching characteristics of NMOS [4] that when gate to source voltage of NMOS is 1.675V then output voltage reaches to zero.

This is the minimum input voltage (V_{IH}) which is recognized by the gate as logic 2.

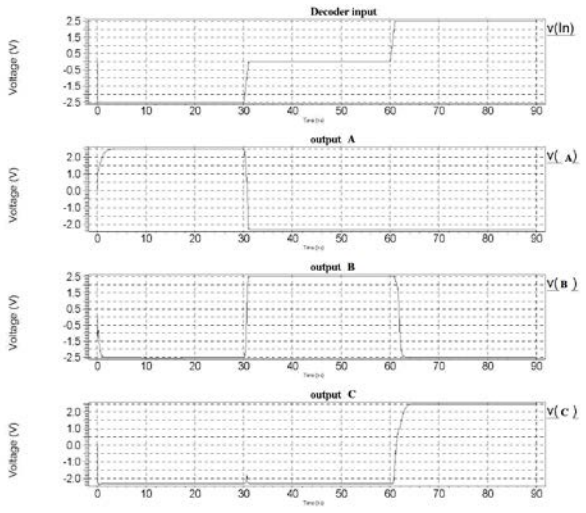

Fig.7.Input and output wavefrom of ternary decoder

5.2 Ternary Multiplexer

Figure 8. represents the circuit schematic of ternary multiplexer using ternary decoder and STNAND gate.Proposed multiplexer is implemented using STNAND gate instead of STNOR [9].Each of the STNAND input is considered as a data input of multiplexer where as decoder input is represented as select line of multiplexer. It can be observed from the input and output waveforms of the STNAND that PMOS and NMOS is used implement the gate follows the exact switching interval during the transition of TRITS input. This property of STNAND is helpful to design the multiplexer for faster switching of the different combination of ternary digits.

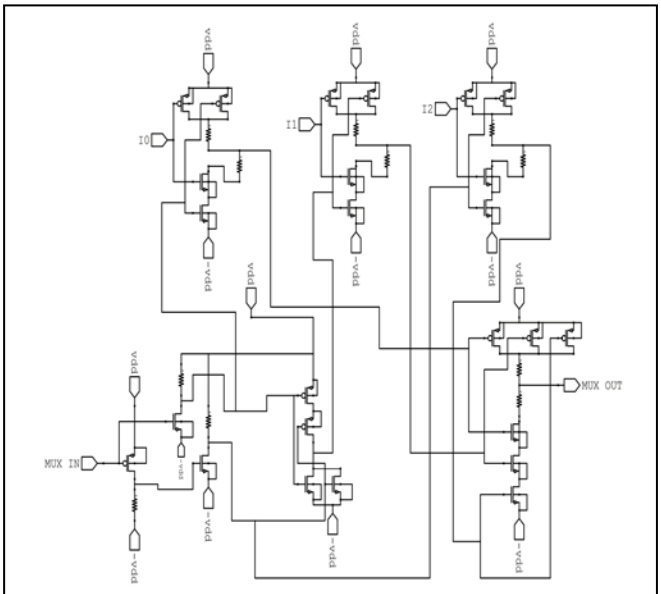

Fig.8.Circuit schematic of ternary multiplexer

Figure.9 represents the ternary multiplexer with select input and data input. Logic 0 (-2.5V) is applied as a select input and 90MHz square wave is applied to data input I_0 . It has been observed from Fig.10 that output of multiplexer follows the exact replica of data input with negligible frequency distortion.This is due to following reason

1.The PMOS and NMOS are used to design the ternary multiplexer also operated in their linear region with a V_{IH}=1.67 volt.

2. There is small amount frequency and phase distortion when data input high time(HT) is taken in between 3ns and 6ns and low time (LT) is taken in between 3ns and 6ns.

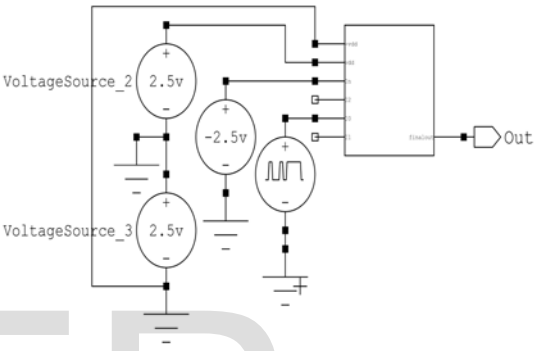

Fig.9.Ternary multiplexer with logic 0 (-2.5V) select i/p and I_0 data i/p

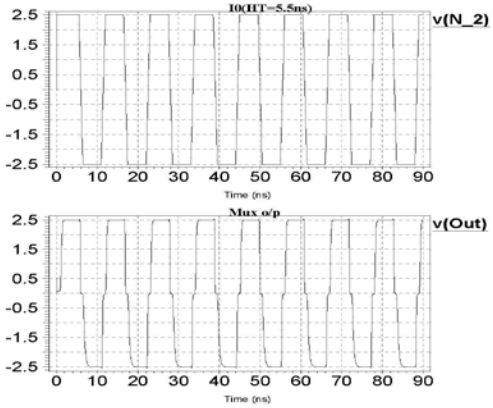

Fig.10 Output waveform of ternary multiplexer with I_0 data i/p of 90MHz.

6. Power Dissipation and Transient Simulation Result of Ternary Logic Gates and Combinational Circuit

The circuits described in the preceding sections have been analyzed using the Tanner EDA tool V.13 with 180nm technology.The average power is measured in the simulation for biasing voltage +VDD=2.5V and –VDD=-2.5V and tabulated

in Table 3 for different types of ternary gates.Power dissipation of ternary combinational circuit is also listed in table 4

TABLE 3
POWER DISSIPATION OF TERNARY LOGIC GATE

Logic Gates	Avg Power (mw)		Total Power (mw)
	$+V_{dd}$	$-V_{dd}$	
NTI	.7168088	.7174644	1.4342732
STI	.1725374	.1731936	0.345731
PTI	.6610104	.6614560	1.322466
NTNOR	.4431646	.4566094	0.899774
STNOR	2.557064	3.231577	5.788641
PTNOR	1.672614	1.686956	3.35957
NTNAND	.8921206	.9066130	1.7987336
STNAND	.1808952	.1826274	0.3635226
PTNAND	.9922072	1.002239	1.9944462

The transient delay analysis of ternary logic gates are illustrated in table.5.The propagation delay (T_{PD}) is calculated after analyzing the T_{PHL} and T_{PLH}.The propagation delay is 629 pico-second due to high speed switching characteristics of PMOS and NMOS transistor.

TABLE 4
POWER DISSIPATION OF TERNARY COMBINATIONAL CIRCUIT

Combinational Circuit	Avg Power (mw)		Total Power (mw)
	$+V_{dd}$	$-V_{dd}$	
Decoder	2.243513	2.244177	4.487690
Multiplexer	1.301587	1.300996	2.602583

TABLE 5
TRANSIENT ANALYSIS

Delay Parameter	Time in Sec
T_{PHL}	6.115e-010
T_{PLH}	6.483e-010
T_{PD}	6.299 e-010
T_{Rise}	3.018e-010
T_{Fall}	3.076e-010

7. CONCLUSION

In this paper the negative, positive and standard ternary logic based inverter, nand gates, nor gates were designed and simulated in a 180 nm technology using Tanner Spice V.13.The circuit schematic of ternary decoder and multiplexer is also implemented using ternary logic gates.The comparative studies of power dissipation of ternary gates and transient delay analysis of combinational circuit has been presented in detail.The ternary multiplexer was created from ternary decoder and SPICE simulation confirmed that correct functional behavior of ternary multiplexer for high speed data switching from data input to output.Future work includes the layout design, area calculation and parasitic extraction and its effect on circuit functionality of ternary logic gates and combinational circuit.

REFERENCES

[1] Balla, P.C.; Antoniou, A., "Low Power Dissipation MOS Ternary Logic Family",IEEE Journal Of Solid-State Circuits, vol. SC-19, no. 5, pp.739-749, 1984.

[2] K.C. Smith, "Multiple-valued logic: A tutorial and appreciation", Computer, vol. 21, no. 4, pp. 17–27, April 1988.

[3] H. T. Mouftah, "A study on the implementation of three-valued logic", Proceedings of the sixth international symposium on Multiple-valued logic (MVL '76). IEEE Computer Society Press, Los Alamitos, CA, USA, 123-126, 1976.

[4] M. Mukaidono, "Regular Ternary Logic Functions Suitable for Treating Ambiguity", IEEE Transactions on Computers,vol.35, no. 2,pp.179-183, February 1986 .

[5] Wu, X.W.; Prosser, F.P., "CMOS ternary logic circuits," Circuits, Devices and Systems, IEE Proceedings G , vol.137, no.1, pp.21-27, Feb 1990.

[6] K.C.Smith, "The prospects for multi valued logic: A technology and applications view", IEEE Trans. Computer.,vol. C-30, pp. 619-634, Sept. 1981.

[7] S.L.Hurst,"Multivalued logic - Its status and its future", IEEE Transactions on Computers, vol. C-33, pp. 1160-1179, 1984.

[8] Sheng Lin; Yong-Bin Kim and Fabrizio Lombardi., "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits",IEEE Trans. on Nanotechnology, vol.10, no.2, pp.217-225, March,2011.

[9] A. Sathish Kumar; A. Swetha Priya., "Minimization of ternary combinational circuits- a survey," International Journal of Engineering Science and Technology, vol. 2(8), pp.3576-3589, 2010.

.